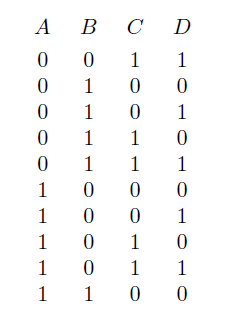
Digital Electronics assignment march 2022

**Question 1**

1. Briefly explain the differences between combinational and sequential logic. [2]
2. With the aid of appropriate diagrams, briey explain the operation of Moore and Mealy finite state machines and highlight their diferences. [6]
3. The state sequence for a binary counter is as follows:



The counter is to be implemented using four synchronously clocked D-type flip flops

1. Draw a state table for the counter, showing the required D inputs. [4]
2. Find expressions for the D inputs, making use of unused states if appropriate. [6]
3. What problem could occur when the counter circuit is powered-up? Give two possible general methods for overcoming the problem. [2]

**Question 2**

1. In a simple copy machine, a stop signal, S, is to be generated to stop the machine operation and energize an indicator light whenever either of the following conditions exists: (1) there is no paper in the paper feeder tray; or (2) the two micro switches in the paper path are activated, indicating a jam in the paper path. The presence of paper in the feeder tray is indicated by a HIGH at logic signal P. Each of the micro switches produces a logic signal (Q and R) that goes HIGH whenever paper is passing over the switch to activate it. Design the logic circuit to produce a HIGH at output signal S for the stated conditions. [10]
2. The notation x1x0 represents a two-bit binary number that can have any value (00, 01, 10, or 11); for example, when x1 = 1 and x0 = 0, the binary number is 10, and so on. Similarly, y1y0 represents another two-bit binary number. Design a logic circuit, using x1, x0, y1, and y0 inputs, whose output will be HIGH only when the two binary numbers x1x0 and y1y0 are equal. [10]

**Question 3**

1. Consider a 4-input Boolean function that outputs a binary 1 whenever an odd number of its inputs are binary 1.
2. Using Boolean logic or otherwise, show how the above function can be implemented using only 2-input XOR gates. [4]
3. Show how the above function may alternatively be implemented using one 4-input decoder, and a minimum number of 4-input NOR and 4-input NAND gates. [3]
4. Consider the following Boolean expression 
5. Show that F can be represented by the following Product of Sums (POS) form  [3]
6. Show how F can be implemented in a 2-level form using OR gates followed by an AND gate. Remember to indicate any NOT gates required, since only uncomplemented input variables are available. [2]
7. Consider your implementation in part b. ii
8. Assume that the gates have finite propagation delay. Describe in detail what happens at the output F when the inputs {A, B, C, D} change from {1, 1, 0, 1} to {1, 1, 1, 1}. [4]
9. Using a Karnaugh map or otherwise, determine the other single input variable change that will give rise to a similar problem to that observed in part (c)(i ). [2]
10. Using a Karnaugh map or otherwise, determine a modied POS expression
11. for F that will eliminate the problems observed in parts (c)(i ) and (c)(ii ) [2]

**Question 4**

1. i. What do you understand by the term multiplexing and state its advantage. [3]

ii. Calculate the number of selection bits required for a multiplexer with 8 data

inputs. [3]

1. A 4 - bit multiplexer is considered to be consisting of two functionally separate

components, a decoder and a combination of switches. The behaviour of the

decoder is summarised by the table below, where S0 and S1 are selection bits,

and D3, D2, D1 and D0 are decoder outputs.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| S0 | S1 | D0 | D1 | D2 | D3 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

i. Design a logic circuit for the decoding component of the multiplexer. [4]

ii. If the data routing is achieved by combining the decoder outputs with the

corresponding inputs (I0, I1, I2, I3) using AND gates, give an expression that will

represent the output of the multiplexer. [2]

iii. Hence, design a logic circuit that combines the decoder outputs with their

corresponding data inputs in order to produce the required output. [4]

**Question 5**

1. Show that
2. (X + Y ).(X + Y ) = X
3. (X + Y ).(X + Z) = (X + Y ).(X + Z).(Y + Z) [5]
4. With the help of the results in part a. or otherwise, simplify the following Boolean expression for W in to a product of sums (POS) form having 3 product terms, each having 3 literals

W = (A + C + F + G).(A + C + F + G).(A + B + C + D + G).(A + C + E + G):(A + B + G).(B + C + F + G) [10]

1. i. Using a Karnaugh map, simplify the following Boolean expression for V into a product of sums (POS) form

V = A.B.C.D + A.B.C.D + (A + B + C + D)

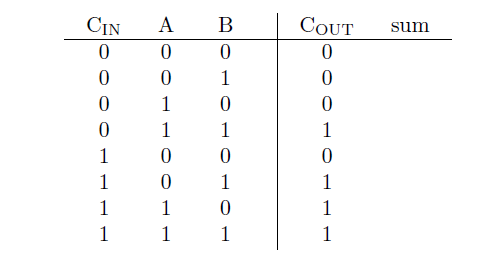
1. Implement the simplified expression for V obtained in Part (c)(i ) using only NOR gates. Assume 2 and 4 input gates are available. Also assume complemented input variables are available. [5]

**Question 6**

1. In a particular computer system, numbers are represented using words having a length of 4 bits.
2. What is the range of positive numbers that can be represented using unsigned binary numbers? [2]
3. Explain how the 2's complement representation can be used to describe signed binary numbers, using 4-bit words as an example. [3]
4. Using decimal (base 10) representation for the answers, perform the following 2's complement 4-bit additions, noting any problems:

* 0110 + 1101 [2]
* 1010 + 1011 [2]

1. Complete the following truth table that describes a single-bit full adder:

[2]

c. Show how 4 single-bit full-adders can be combined to implement a 4-bit ripple carry-adder. [2]

d. Briefly describe how the speed of operation of the approach in part (c) could be improved. [4]

e. Show how COUT in part (b) can be implemented using only NAND gates [3]